A Review of Solid State Transistor Technologies for future low power high speed and high power applications

D. Nirmal*

Department of Electronics and Communication Engineering
Karunya Institute of Technology and Sciences
Coimbatore, Tamilnadu, India

Received 17 June 2020

Abstract: In this review article, solid state transistor technologies for high speed, high power and low power applications are studied. The significance of nanowire (NW) MOSFETs, FinFETs, Junctionless transistor, double gate MOSFETs, Tunnel field effect transistors (TFETs) and also materials for low power applications have been intensively studied. The suitability of InP HEMTs for high speed applications and AlGaN/GaN HEMTs for high power applications have also been systematically analyzed. The impact of various high-K dielectric materials on the on and off state performance of low power transistors also been investigated. This review article also highlights the influence of scaling on the RF and DC performance of solid state transistors for low power, high speed, and high power applications. Finally, the effect of field plates and passivation techniques on the breakdown performances of high electron mobility transistors (HEMTs) have also been systematically studied.

Keywords: Double gate MOSFETs, Nanowire MOSFETs, FinFETs, TFETs, Junctionless Transistor, InP HEMT, GaAs MHEMT and AlGaN/GaN HEMT.

1 Introduction

In the present nano period, semiconductor transistors have been downscaled constantly to accomplish great speed and high packing density with superior device

*Recipient of Dr. M. Anandakrishnan Prize: Young Scientist Award in Engineering and Technology (2019); E-mail: dnirmalphd@gmail.com

performance. In any case, this scalingdown of geometrical dimensions of semiconductor device prompts the unfortunate short channel impacts such as, high leakage current, drain induced barrier lowering DIBL and threshold voltage roll off (Vt roll off) is the hindrance for the circuit designers. Hence, the opportunity to consider the other novel device structures and materials for future RF and microwave applications. TFETs have risen as compromising alternate device for future low power logic applications due to their distinct advantages of low sub- threshold swing (SS) and high Ion/Ioff ratio. Additionally, the exhibition of TFETs isn't impacted by short channel effects (SCE) because of the nearness of the tunnelling barrier width. TFETs with various materials like Si, SiGe, III-V, Ge have likewise to improve the drain current.

The SiO_2 has been used in traditional CMOS devices for years. However, the limitations of the SiO_2 are a critical issue for future high speed low power applications. Moreover, the short channel effects and the gate leakage have been considered as the major threats in traditional semiconductor transistors due to the destitute scaling limit (less than 10 nm). Usually, the leakage current decreases exponentially when the thickness of the gate oxide increases, leading to poor performance of conventional CMOS devices. To address these issues, many researchers have been experimenting new gate oxides such as Al_2O_3, ZrO_2 and HfO_2 as gate dielectrics.

The most recent decade has seen a blast of enthusiasm for rapid transistors reasonable for low power and high speed applications. InGaAs based High Electron Mobility Transistors (HEMTs) and hetero-junction bipolar transistors (SHBTs and DHBTs) have demonstrated gigantic achievement in millimeter, sub-millimeter and microwave applications, and accordingly these transistors have been considered as the potential answers for the coming days' terahertz (THz) applications. The transistors with outstanding DC/RF exhibitions have been accomplished through utilization of high electron mobility channel material having more sheet charge densities, the blend of decrease in parasitic and furthermore through the downscaling of devices to least element size. Modern day work at E-Mode InAlAs/ InGaAs HEMTs on Indium phosphide wafer have shown prevalent low-noise, higher level gain and high-frequency exhibitions over HEMTs on some other material frameworks, for example, GaAs, and this is mostly because of the high electron transport properties, for example, higher electron motilities, high immersion speeds and good sheet charge densities (2DEG) of the InGaAs channel. However, MMICs on GaAs wafers and transistors have become necessary components in low-commotion business with wide data transfer capacity remote correspondence frameworks. Because of the huge expense of InP wafer, InP-based transistors and MMICs have not encountered a comparative interest and development. Metamorphic HEMTs (MHEMTs) on GaAs wafer are getting progressively famous for the assembling of MMICs and TMICs for high-power and low noise applications since

these device give numerous favourable circumstances, for lower wafer cost because of greater mechanical strength, huge volume manufacturing, matured processing technology with a 6-in Gallium Arsenide wafer.

GaN HEMTs are highly preferable for microwave and radio frequency applications because of unique wide band gap properties. AlGaN/GaN build HEMTs can deliver a favourable on resistance, frequency, break down field, power compared with the traditional Si and SiC based transistors for Radio Frequency power applications. However, in order to increase the operating frequency, it is essential to reduce the thickness of AlGaN barrier layer which in turn maximize short channel effects.

2 Solid state transistors for low power applications

In 2012, a nanoscale double gate MOSFET with channel engineering technique have been demonstrated for mixed signal applications [1]. Double gate MOSFETs with gate dielectric materials having high permittivity exhibited the low off current. For double gate MOSFETs with high k dielectric gate oxides, the DIBL decreases with increase in permittivity of gate dielectrics and it is also proved that the Ion/Ioff ratio increases with increase in permittivity of the gate dielectric. The switching performance of CMOS inverter has also been investigated in [1] using double gate MOSFET. In 2016, a novel dual metal gate engineered nanowire MOSFET has been demonstrated using different dielectric materials for low power applications [2]. The structure of dual metal gate engineered nanowire MOSFET is shown in Fig. 1. DMSGJLT with SiO_2 dielectric exhibited the highest on current compared with high-k dielectric materials such as Si_3N_4, Al_2O_3, TiO_2, Y_2O_3 and HfO_2. However, DMSGJLT with high-k gate oxides exhibited high Ion/Ioff ratio and low DIBL compared with SiO_2 dielectric. CMOS inverter designed with DMSGJLT having high-K dielectric gate oxides dissipates less power compared with SiO^2 dielectric based DMSGJLT.

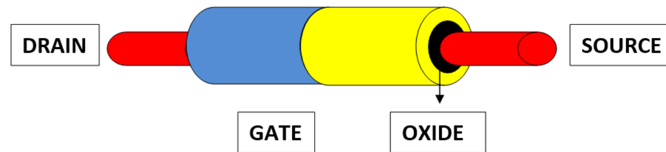

Fig. 1: Dual metal surround gate junction less transistor (DMSGJLT)

In 2010, ZrO_2 nanoparticle has been synthesized at room temperature for nanoscale FinFETs using wet chemical methods [2]. In 2011, the analog and RF performance

of FinFETs using high-k dielectrics have been investigated, FinFET with ZrO_2 dielectric exhibited higher transconductance, on current and low off current compared with FinFETs with SiO_2, Si_3N_4 and Al_2O_3 gate dielectrics [3]. FinFETs with ZrO_2 exhibited higher transit frequency and lower channel resistance compared with SiO_2, Si_3N_4 and Al_2O_3 gate dielectric based FinFETs. In 2013, the subthreshold performance of a CMOS inverter designed with gate engineered and high-k dielectric based FinFETs (Fig. 2) have been investigated using TCAD tool and found that high-k dielectrics in FinFETs improves the switching performance of the CMOS inverter due to low DIBL, high on current, low off current, high Ion/Ioff current ratio and high transconductance generation factor.

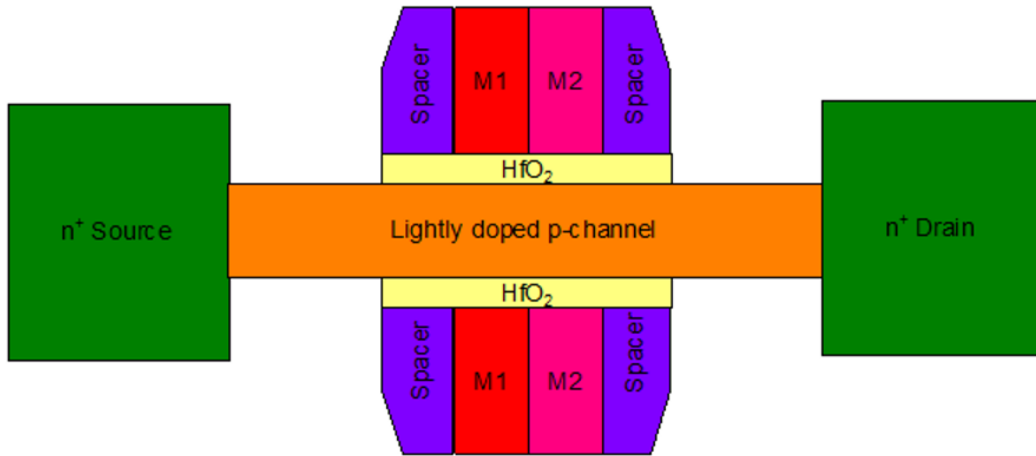

Fig. 2: Gate engineered and high-k dielectric based FinFETs

In 2015, I-V characteristics of triple material gate stack gate all-around (TMGS-GAA) MOSFET has numerically modelled by considering quantum mechanical ef fects. In 2016, the Drain Current of a Dual Metal Junctionless Transistor is mathematically modelled [2]. In 2017, the influence of various high-K dielectric based nanoscale junctionless transistor on the performance of 6T SRAM circuit is investigated and found that the 6T SRAM circuit (Fig. 3) executed shows highest improvement in read noise margin for HfO_2 than SiO_2. This also shows improvement in hold noise margin and in write noise margin for HfO_2 than SiO_2. [4].

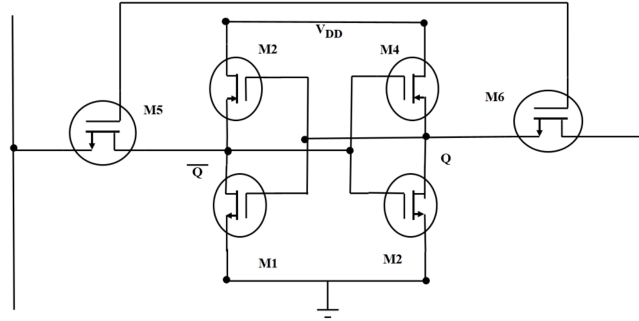

Fig. 3: 6T SRAM designed using nanoscale Junctionless transistor

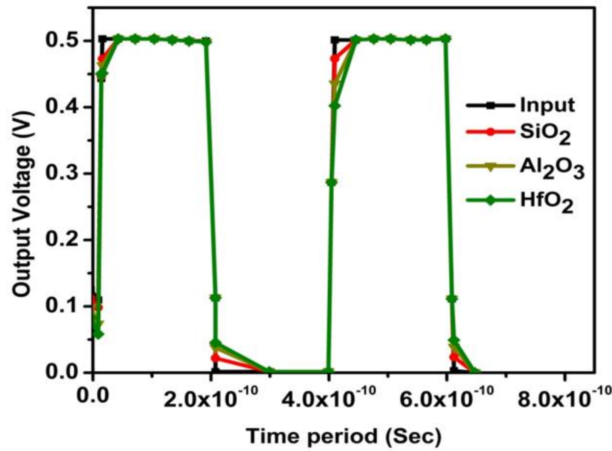

Fig. 4: Input/Output characteristics of 6T-SRAM designed using Junctionless transistor

In 2017, to overcome the issues in traditional Si based TFET, Germanium based dual metal DG TFET device has been investigated. Ge based TFET offers a good drive current and enhanced Subthreshold slope using Ge channel. It has minimum leakage current ($9.27\text{x}10^{-13}$ A/μm), a more on current ($1.3\text{x}10^{-4}$ A/ μm), giving good Subthreshold slope of 34 mV/dec. This indicates DG TFET is good for low power applications. In 2019, a novel Dual Material Double Gate TFET (DMDGTFET) with reduced high-K dielectric length and drain electrode thickness is investigated using TCAD tool [5]. In 2019, the performance of a triple material double gate TFET is enhanced by using a combination of heterojunction and high-k dielectrics [7].

3 Solid state transistors for high power applications

In the coming years, improvement in fabrication technology and its high frequesny properits, GaN material is suitable for future power-electronic devices. In 2015, the impact of high-k passivation layer on break- down characteristics of Schottky AlGaN/GaN HEMTs have been investigated using TCAD tools and observed that HEMT with a Lgd of 1.5 μm and with high-k passivation layer gives a high Off-state breakdown voltage. In 2017, the current collapse in AlGaN/GaN HEMT withheld plate engineering is investigated. This analytical model is useful to correlate the impact in intrinsic capacitance and conductance. The new device minimizes the current collapse phenomena by 10% compared with the traditional AlGaN/GaN HEMTs. Moreover, the device exhibited a drain current of 900mA/mm, breakdown voltage of 291 V and transconductance of 175 mS/mm [6]. The schematic of field plated AlGaN/GaN HEMT is shown in Fig. 5. In 2018, the RF and DC characteristics of AlGaN/GaN HEMT is improved by using discrete field plate technique. The discrete field plate minimizes the electric field between gate and drain to obtain the breakdown voltage of 330 V. The field-plates enhance the DC characteristics by reducing the currents developed near the gate region.

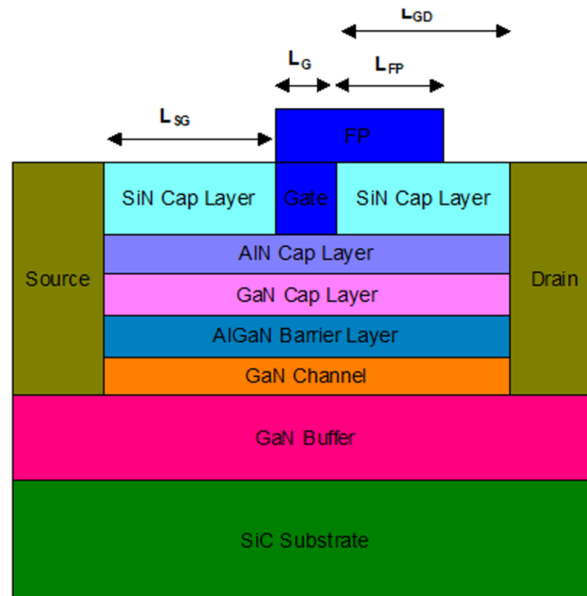

Fig. 5: Cross sectional schematic of field plated AlGaN/GaN HEMT

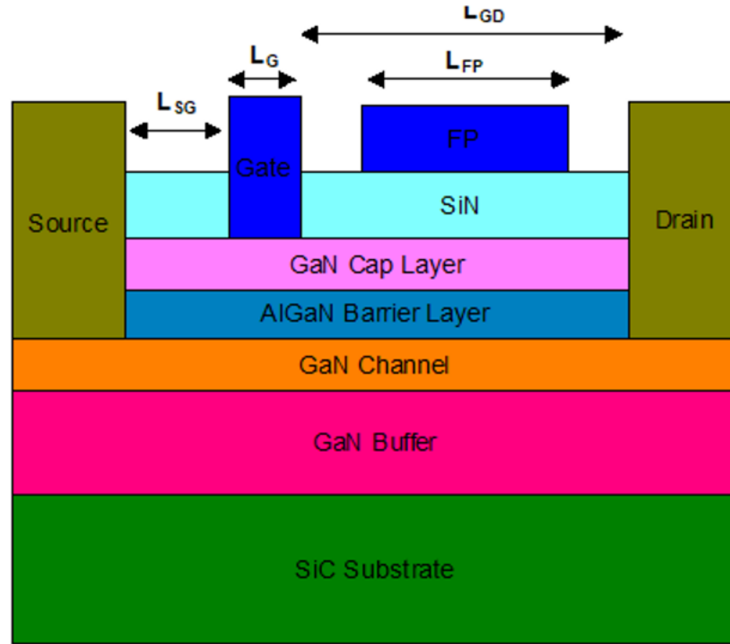

Fig. 6: AlGaN/GaN HEMT with discrete field plate

The combination of discrete field plate and AlGaN blocking layer is found to be effective in improving the Johnson figure of merit of AlGaN/GaN HEMTs [7]. The RF and DC performance in AlGaN/GaN HEMT can be improved by P-type doping in GaN buffer for mm-wave applications [8]. GaN based HEMT on Silicon Carbide (SiC) wafer is good alternate for microwave and power switching systems.

4 Solid state transistors for high speed applications

Indium phosphide is a material which has an ability for applications in high speed internet access, satellite communications, video conferencing, real time multimedia transfer and high speed electronics because of its higher velocity of saturation, high sheet electron densities and high room temperature electron mobility. There has been impressive enthusiasm for creating Indium phosphide based transistors, for HEMTs, HBTs and MOSFETs utilizing different innovations, for Gate/Drain/Source engineering since the time a few focal points of the inborn properties like high thermal conductivity, low voltage operation and high electron mobility, so as to pick up favorable circumstances over Silicon, SiGe and GaAs build

semiconductor. Ongoing advances of Indium phosphide based transistors, make them appealing contender for key segments in IC applications. Despite the fact that its widespread use has been limited in applications with more elevated level of integration because of its low process yield and in this manner significant expense. The QW-MOSFET with Al_2O_3/ZrO_2 heterodielectric exhibited superior mobility, gate leakage, subthreshold current, transconductance, drain current and reduced short channel effects compared with QW-MOSFET with single gate dielectric such as Al_2O_3 and HfO_2.

In 2016, the DC and RF execution of a SiN passivated 20 nm gate length MHEMT on GaAs wafer with doped InGaAs source/channel (S/D) regions have explored utilizing the Synopsys TCAD instrument. This MHEMT additionally includes δ-doped sheets on either side of the In0.53Ga0.47As/InAs/In0.53Ga0.47As channel which shows a trans conductance cut off recurrence (fT) of 740 GHz and also of 3100 mS/mm. It posses 1040 GHz of most extreme wavering recurrence (fmax). The gadget is seen 0.07V as The threshold voltage with the 2DEG measuring around 12600 cm^2/Vs at hall room temperature with a sheet charge thickness bigger than 3.6x1012 cm^2. In 2016, The DC and RF performance of E-Mode In0.7Ga0.3As/InAs/ In0.7Ga0.3As composite channel HEMT on InP wafer with doped In0.52Ga0.48As S/D Lg=20 nm regions is compared with conventional HEMT structure.

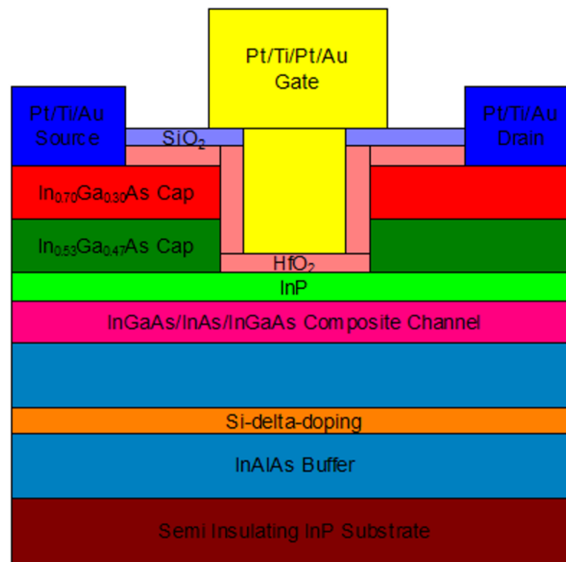

Fig. 7: Schematic of In0.53Ga0.47As/InAs/In0.53Ga0.47As Composite Channel QW-MOSFET

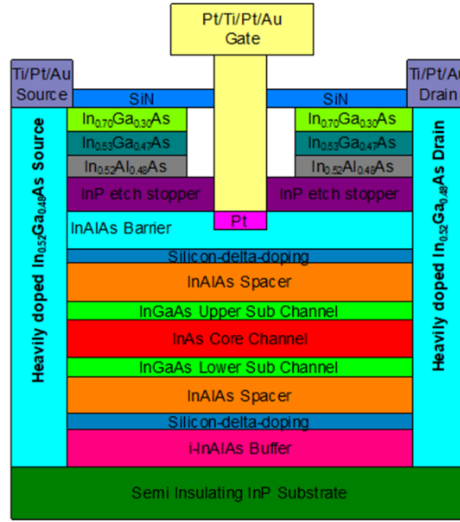

Fig. 8: InP HEMT structure

This device also features double d-doping technology, multilayer cap, T-gate and thin layer of platinum embed into the barrier layer. This exhibited 15% improvement in drain current compared to traditional HEMT device with a 14% improvement in transconductance (gm). Additionally this new device shows 17% improvement in maximum oscillation frequency (fmax) and 25% improvement in cut off frequency (fT) contrasted with traditional HEMT structure and this magnificent presentation is accomplished chiefly because of the low gate length and furthermore also because of the decrease of parasitics, with source and drain resistance . In 2016, a 20-nm T-gate channel E-Mode MHEMT on GaAs wafer for future THz applications were studied using TCAD tool [9]. The DC characteristics of this MHEMT is plotted in Fig. 9.

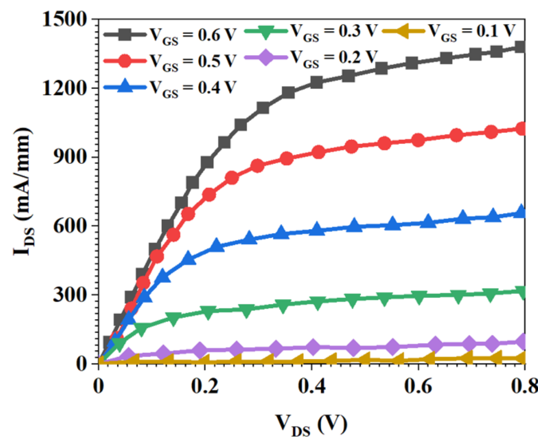

Fig. 9: Output curves of MHEMT

In 2019, the impact of gate underlap and overlap of the DC/RF properties of a composite channel DG MOSFET is suggested for RF/analog applications. TCAD simulations shows improvement in the analog and RF performance of the DG MOSFET by reducing the Lg and employing a gate underlap strategy technique. In 2019, Next Generation High Speed Low Power Applications have been experimented with a new 20 nm High Performance GaAs Substrate Based Metamorphic MOSHEMT [10-11]. The influence of different dielectric passivation materials such as SiO_2, Si_3N_4, Al_2O_3 and Si_3N_4/Al_2O_3 on the DC & RF performance of InP-HEMT was analyzed using TCAD tool [12]. This InP HEMT provides a Pt sinking technology with T-Gate structure to suppress SCEs, n+-doped In0.52Ga0.48As drain-source areas are reduced the D/S parasitic resistance and the 2-dimensional charge density in the quantum well enhanced by double-Si--doping technique. Indium phosphide HEMT is observed as one of the best transistor technology for future optical communication & high speed wireless communications, high speed IC applications, sensing & imaging and radiometry & deep space communication systems.

5 Conclusion

In this review article, the solid state transistor technologies for future low power high speed and high power applications have been studied intensively. Even though FinFET is considered as an attractive transistor technology for the present high speed low power applications, nanowire or nanosheet junctionless transistor technologies will take over beyond 5 nm node. GaN HEMTs will continue in the main steam for high power applications along with SiC MOSFETs due to its wideband gap properties. InP HEMTs and GaAs MHEMTs have been considered as the most preferable solid state transistor technologies for future high speed applications due to their high Ft and fmax of over 700 GHz and 1THz respectively.

References

1. D Nirmal, P Vijayakumar, K Shruti and N Mohankumar, " Nanoscale channel engi- neered double gate MOSFET for mixed signal applications using high-k dielectric", Int. J. Circ. Theor. Appl. (2012).

2. J. Charles Pravin, D. Nirmal, P. Prajoon, and M. Anuja Menokey, "A New Drain Current Model for a Dual Metal Junctionless Transistor for Enhanced Digital Circuit Performance", IEEE Transactions On Electron Devices, VOL. 63, NO. 9, SEPTEM- BER 2016.

3. Chang-Woo Sohn ; Chang Yong Kang ; Rock-Hyun Baek ; Do-Young Choi ; Hyun Chul Sagong ; Eui-Young Jeong ; Chang-Ki Baek ; Jeong-Soo Lee ; Jack C. Lee ; Yoon-Ha Jeong, “Device Design Guidelines for Nanoscale FinFETs in RF/Analog Applications”, IEEE Electron Device Letters, Vol. 33, No. 9, P. 1234-1236, 2012.

4. J. Charles Pravin, D. Nirmal, P. Prajoon, N. Mohan Kumar, J. Ajayan, “Investi- gation of 6T SRAM memory circuit using high-k dielectrics based nano scale junc- tionless transistor”, Superlattices and Microstructures 104 (2017) 470e476.

5. Sanjay Kumar ; Ekta Goel ; Kunal Singh ; Balraj Singh ; Prince Kumar Singh ; Kamalaksha Baral ; Satyabrata Jit, “2-D Analytical Modeling of the Electrical Characteristics of Dual-Material Double-Gate TFETs With a SiO2/HfO2 Stacked Gate-Oxide Structure”, IEEE Transactions on Electron Devices, Vol. 64, No. 3, P. 960-968, 2017.

6. D. Nirmal, L. Arivazhagan, A.S.Augustine Fletcher, J. Ajayan, P. Prajoon, “Current collapse modeling in AlGaN/GaN HEMT using small signal equivalent circuit for high power application”, Superlattices and Microstructures xxx (2017) 1e11.

7. Dilder Chowdhury, “Power Gallium Nitride Technology: The Need for Efficient Power Conversion”, IEEE Electrification Magazine, Vol. 8, No. 2, P. 6-10, 2020.

8. Benoit Bakeroot ; Arno Stockman ; Niels Posthuma ; Steve Stoffels ; Stefaan De- coutere, “Analytical Model for the Threshold Voltage of p -(Al)GaN High-Electron- Mobility Transistors”, IEEE Transactions on Electron Devices, Vol. 65, No. 1, P. 79-86, 2018.

9. J. Ajayan, D. Nirmal, “20-nm T-gate composite channel enhancement-mode meta- morphic HEMT on GaAs substrates for future THz applications”, J Comput Elec- tron DOI 10.1007/s10825-016 0884-4, 2016.

10. Qiang Li ; Xiuju Zhou ; Chak Wah Tang ; Kei May Lau, “High-Performance Inverted In0.53Ga0.47As MOSHEMTs on a GaAs Substrate With Regrown Source/Drain by MOCVD”, IEEE Electron Device Letters, Vol. 33, No. 9, P. 1246-1248, 2012.

11. Qiang Li ; Xiuju Zhou ; Chak Wah Tang ; Kei May Lau, “Material and Device Characteristics of Metamorphic In0.53Ga0.47As MOSHEMTs Grown on GaAs and Si Substrates by MOCVD”, IEEE Transactions on Electron Devices, Vol. 60, No. 12, P. 4112-4118, 2013.

12. Peng Ding ; Chen Chen ; Muhammad Asif ; Xi Wang ; Jiebin Niu ; Feng Yang; Wuchang Ding ; Yongbo Su ; Dahai Wang ; Zhi Jin, “Si_3N_4/Al_2O_3 Stack Layer Passivation for InAlAs/InGaAs InP-Based HEMTs With Good DC and RF Performances”, IEEE Journal of the Electron Devices Society, Vol. 6, P. 49-54, 2018.